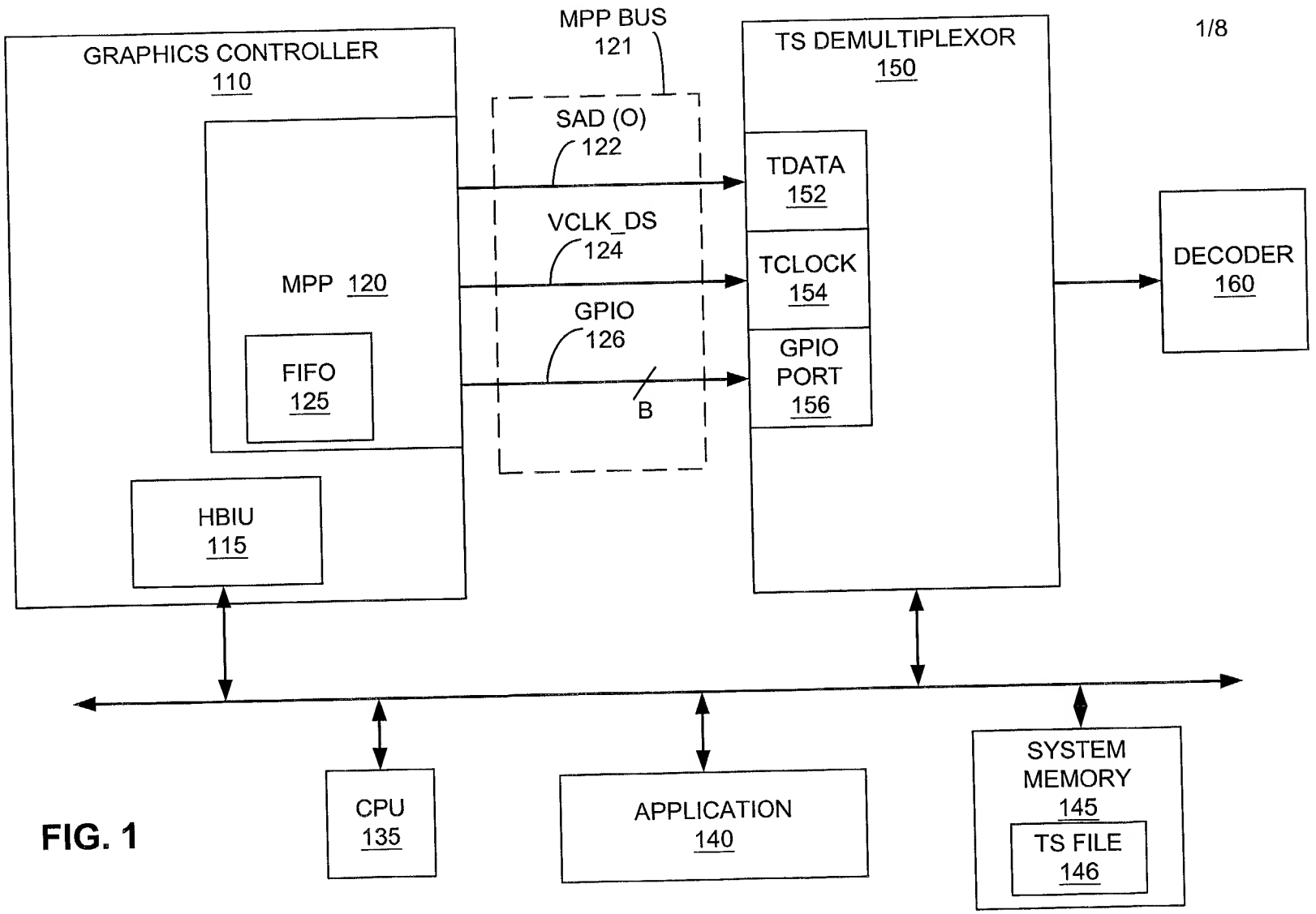

FIG. 1

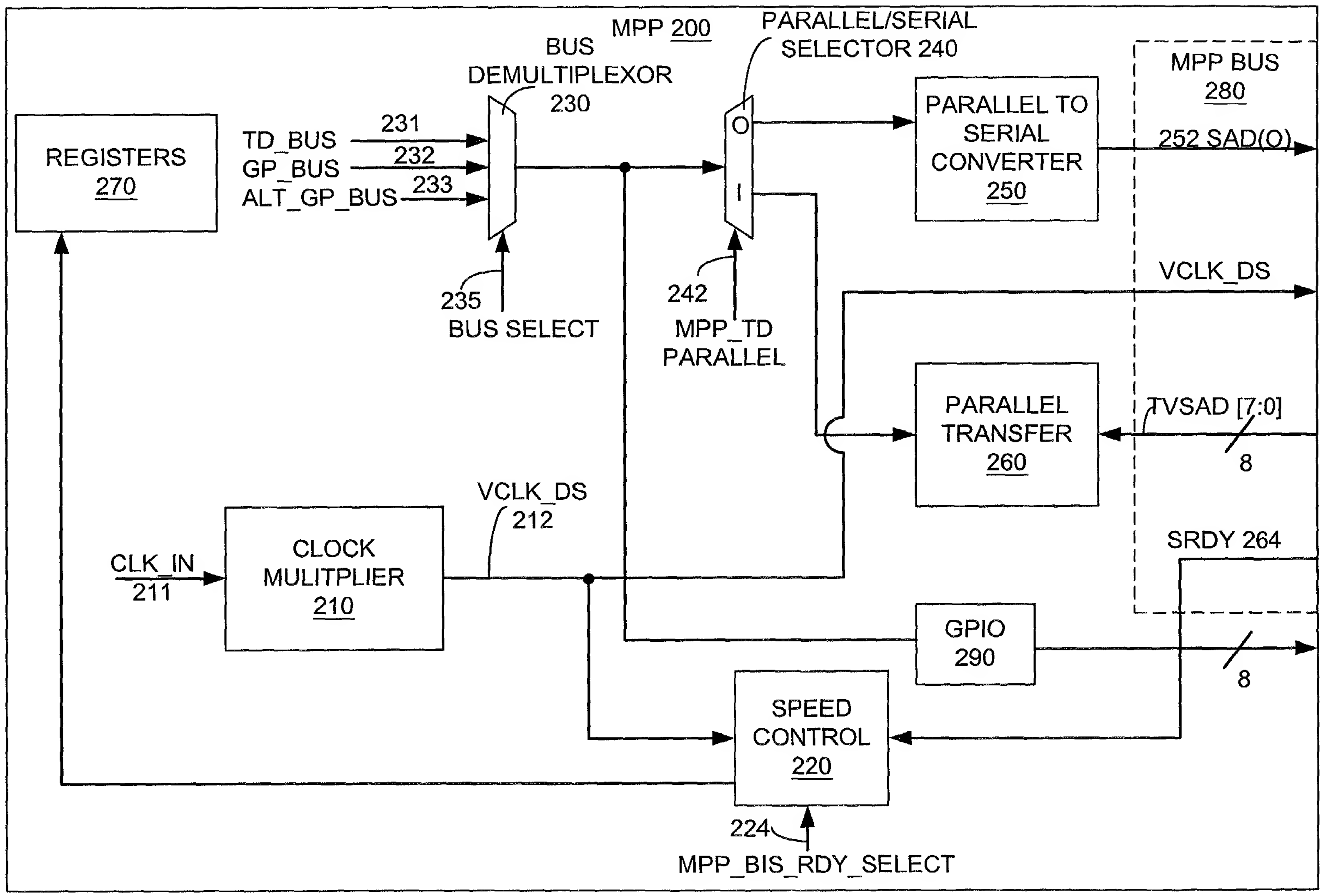
MPP 200
BUS
DEMULTIPLEXOR
230
PARALLEL/SERIAL
SELECTOR 240
MPP BUS
280
REGISTERS
270
TD_BUS
GP_BUS
ALT_GP_BUS
231
232
233
O
I
PARALLEL TO
SERIAL
CONVERTER
250
252 SAD(O)
235
BUS SELECT
242
MPP_TD
PARALLEL
VCLK_DS
PARALLEL
TRANSFER
260
TVSAD [7:0]
8
VCLK_DS
212
CLK_IN
211
CLOCK
MULITPLIER
210
SRDY 264
GPIO
290
8
SPEED
CONTROL
220
224
MPP_BIS_RDY_SELECT

FIG. 2

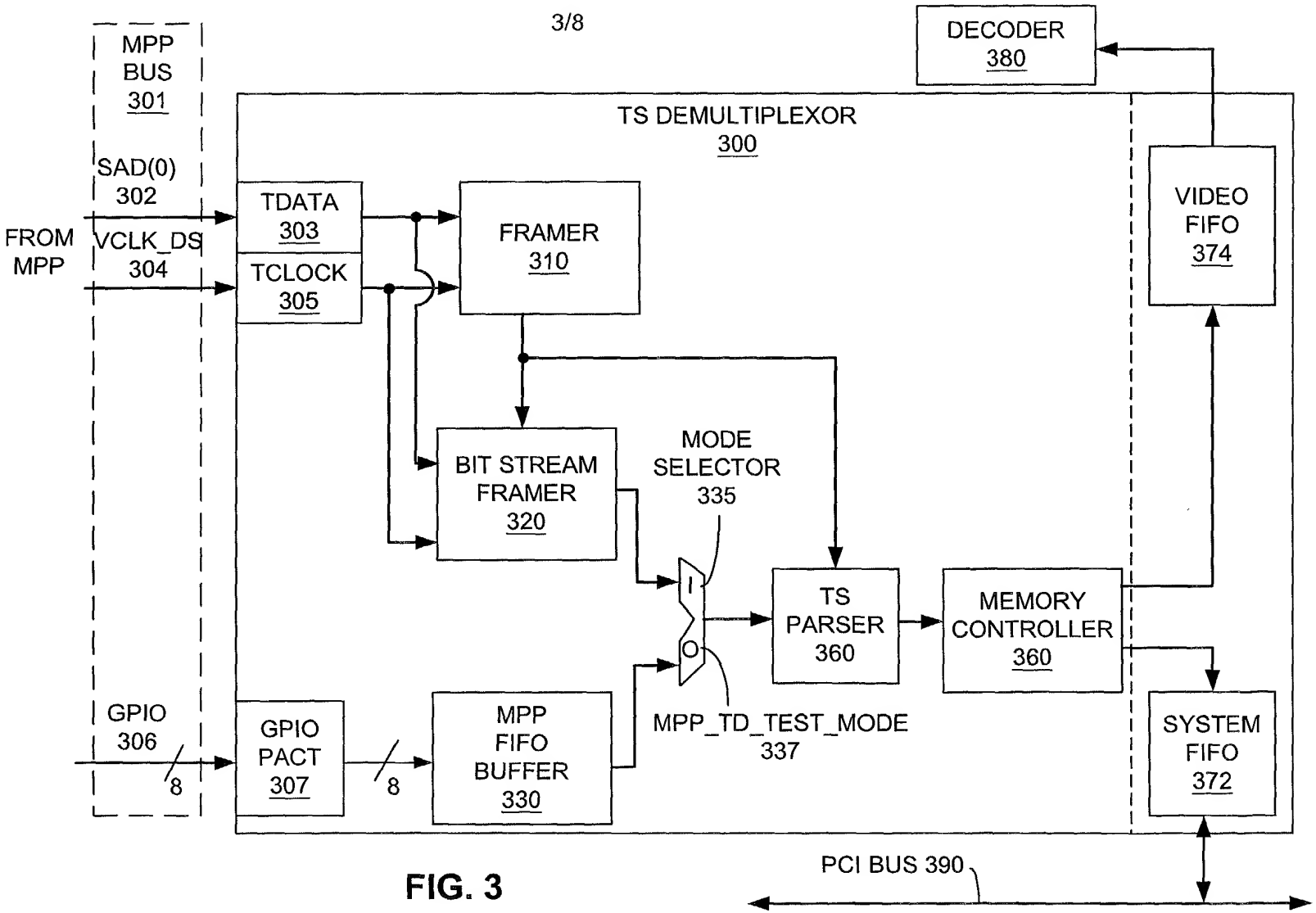
DECODER
380
TS DEMULTIPLEXOR
300
MPP
BUS
301
SAD(0)
302
FROM
MPP
VCLK_DS
304
TDATA
303
TCLOCK
305
FRAMER
310
VIDEO
FIFO
374
BIT STREAM
FRAMER
320
MODE
SELECTOR
335
I
O
TS
PARSER
360
MEMORY
CONTROLLER
360
GPIO
306
8
GPIO
PACT
307
8
MPP
FIFO
BUFFER
330
MPP_TD_TEST_MODE
337
SYSTEM
FIFO
372
PCI BUS 390

FIG. 3

MPP_GP_CONFIG MMR:0x08C8 IND:0x08C8 [RW] 32 bits			
Field Name	**Bits**	**Default**	**Description**
MPP_GP_ALT_REG_EN	3	0x0	The enable bit for the MPP_ALT_REG mode, for register based streaming into the demux framer.
MPP_GP_EN	31	0x0	0=Disable MPP; 1=Enable MPP master.

MPP_CLK_CNTL MMR:0x0074 IND:0x0074 [RW] 32 bits (access: 32)			
Field Name	**Bits**	**Default**	**Description**
MPP_CLK_FRACTION	11:0	0x0	Controls the data rate. The higher value it is set to, the faster MPP sends data to TD
MPP_BUSRDY_SELECT	28	0x0	0 - normal MPP busrdy signal is used; 1 - special MPP busrdy signal is used. This is used to control the rate for MPP sends data to TD
MPP_TDTEST_MODE	29	0x0	0 - Send data to SAD; 1 - Send data to TD through GPIO bus
MPP_TD_PARALLEL	31	0x0	0 - send serial stream to TD; 1 - send 8 bit parallel stream to TD

MPP_GP_ALT_REG_ADDR MMR:0x0088 IOR:0x0088 IND:0x0088 [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
MPP_GP_ALT_REG_AD	7:0	0x0	The address of the register that MPP will write/read when MPP is in the ALT_REG mode. Only the lowest byte is used, and no byte write should be done on the upper 3 bytes.

MPP_GEN_STATUS MMR:0x008C IOR:0x00F4 IND:0x00F4 [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
MPP_TD_RDY (read)	0	0x0	0=MPP_TD_BUS_RDY; 1=MPP_TD_BUS_BUSY
MPP_GP_RDY (read)	1	0x0	0=MPP_GP_BUS_RDY; 1=MPP_GP_BUS_BUSY
MPP_GP_ALT_RDY (read)	2	0x0	0=MPP_GP_ALT_BUS_RDY; 1=MPP_GP_ALT_BUS_BUSY
MPP_GP_INT_FLAG (read)	3	0x0	0=MPP no MPP interrupt;1=MPP interrupt from TD, GP or ALT_GP bus.

AMCGPIO_MASK MMR:0x08B0 IND:0x08B0 [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_MASK	31:0	0x0	0=shared by VIP, MPP,I2C, TD, or I2S bus; 1=GPIO pin only.

AMCGPIO_A_REG MMR:0x08B4 IND:0x08B4 [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_A	31:0	0x0	Input from GPIO bus – read status from input pins

AMCGPIO_Y_REG MMR:0x08B8 IND:0x08B8 [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_Y (R)	31:0	0x0	Input to GPIO bus – write data to output pins

AMCGPIO_EN_REG MMR:0x08BC IND:0x08BC [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_EN	31:0	0x0	0=input direction.; 1=output direction.

FIG. 4A

MPP_GP_CONFIG [RW] 32 bits			
Field Name	**Bits**	**Default**	**Description**
MPP_GP_ALT_REG_EN	3	0x0	The enable bit for the MPP_ALT_REG mode, for register based streaming into the demux framer.
MPP_GP_EN	31	0x0	0=Disable MPP; 1=Enable MPP master.

MPP_CLK_CNTL [RW] 32 bits (access: 32)			
Field Name	**Bits**	**Default**	**Description**
MPP_CLK_FRACTION	11:0	0x0	Controls the data rate. The higher value it is set to, the faster MPP sends data to TD
MPP_BUSRDY_SELECT	28	0x0	0 - normal MPP busrdy signal is used; 1 - special MPP busrdy signal is used. This is used to control the rate for MPP sends data to TD
MPP_TDTEST_MODE	29	0x0	0 - Send data to SAD; 1 - Send data to TD through GPIO bus
MPP_TD_PARALLEL	31	0x0	0 - send serial stream to TD; 1 - send 8 bit parallel stream to TD

MPP_GP_ALT_REG_ADDR 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
MPP_GP_ALT_REG_AD	7:0	0x0	The address of the register that MPP will write/read when MPP is in the ALT_REG mode. Only the lowest byte is used, and no byte write should be done on the upper 3 bytes.

MPP_GEN_STATU [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
MPP_TD_RDY (read)	0	0x0	0=MPP_TD_BUS_RDY; 1=MPP_TD_BUS_BUSY
MPP_GP_RDY (read)	1	0x0	0=MPP_GP_BUS_RDY; 1=MPP_GP_BUS_BUSY
MPP_GP_ALT_RDY (read)	2	0x0	0=MPP_GP_ALT_BUS_RDY; 1=MPP_GP_ALT_BUS_BUSY
MPP_GP_INT_FLAG (read)	3	0x0	0=MPP no MPP interrupt;1=MPP interrupt from TD, GP or ALT_GP bus.

AMCGPIO_MASK [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_MASK	31:0	0x0	0=shared by VIP, MPP,I2C, TD, or I2S bus; 1=GPIO pin only.

AMCGPIO_A_REG [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_A	31:0	0x0	Input from GPIO bus – read status from input pins

AMCGPIO_Y_REG [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_Y (R)	31:0	0x0	Input to GPIO bus – write data to output pins

AMCGPIO_EN_REG [RW] 32 bits (access: 8/16/32)			
Field Name	**Bits**	**Default**	**Description**
AMCGPIO_EN	31:0	0x0	0=input direction.; 1=output direction.

FIG. 4B

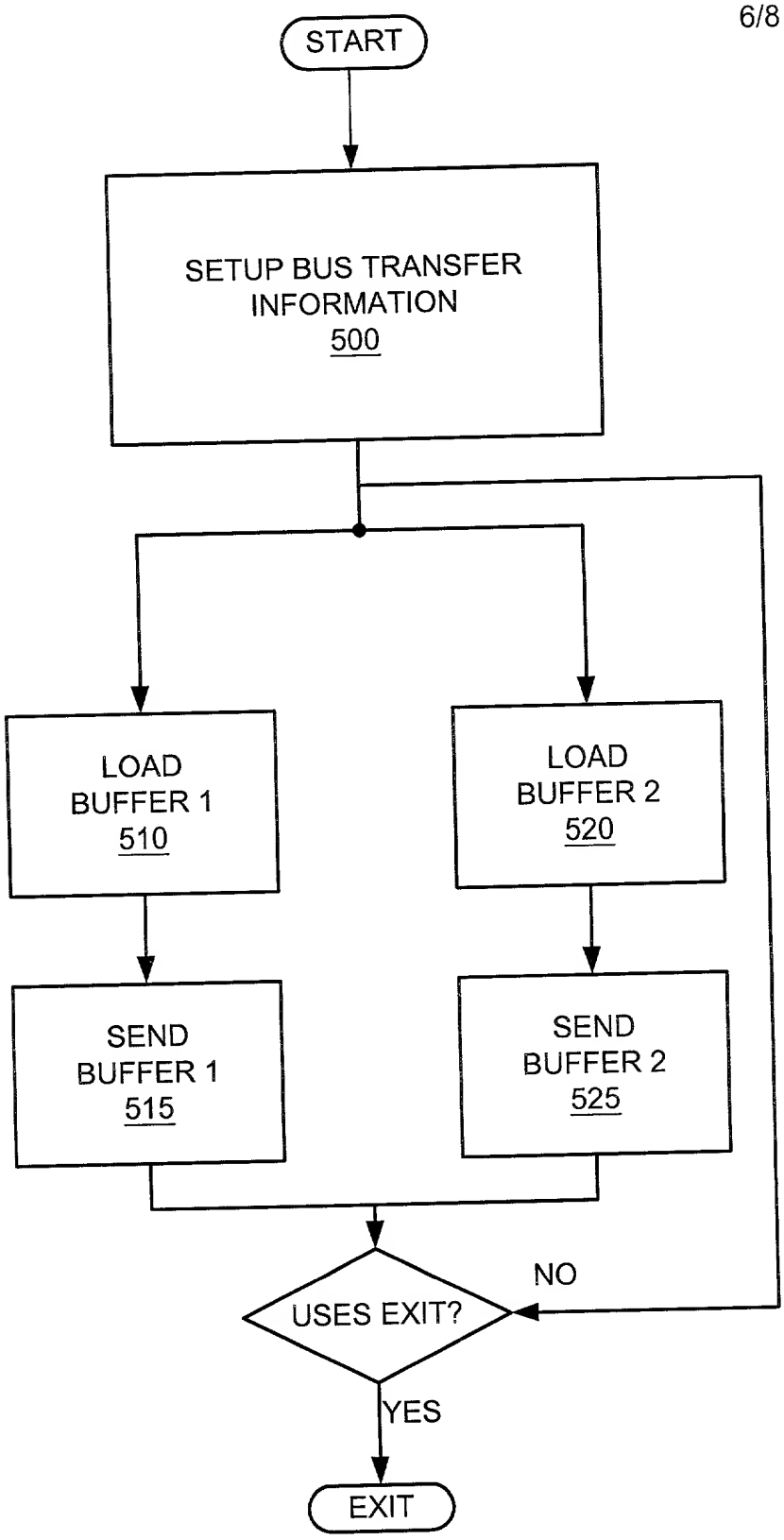

FIG. 5

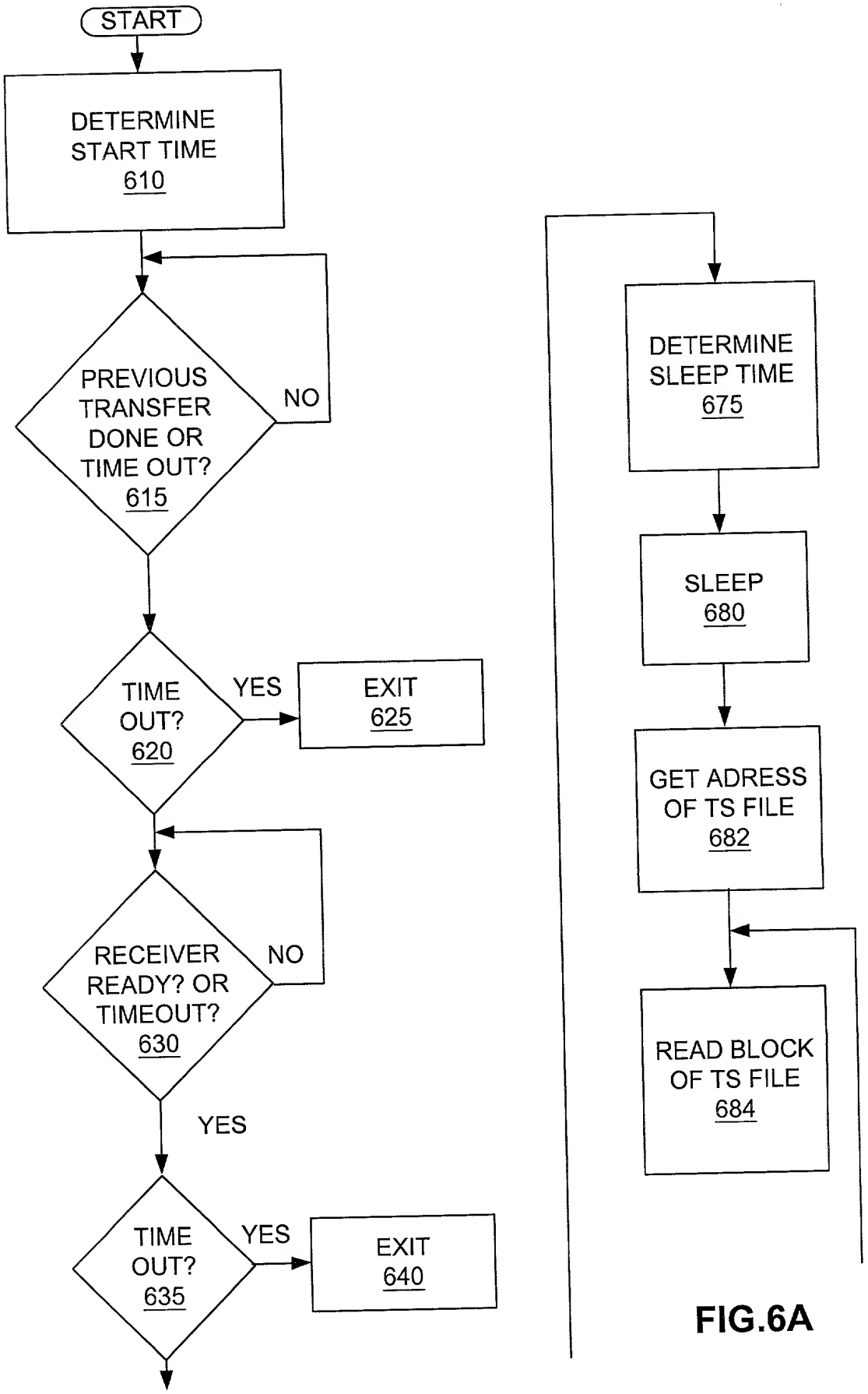
START
DETERMINE START TIME 610
PREVIOUS TRANSFER DONE OR TIME OUT? 615
NO
TIME OUT? 620
YES
EXIT 625
RECEIVER READY? OR TIMEOUT? 630
NO
YES
TIME OUT? 635
YES
EXIT 640
DETERMINE SLEEP TIME 675
SLEEP 680
GET ADRESS OF TS FILE 682
READ BLOCK OF TS FILE 684

FIG.6A

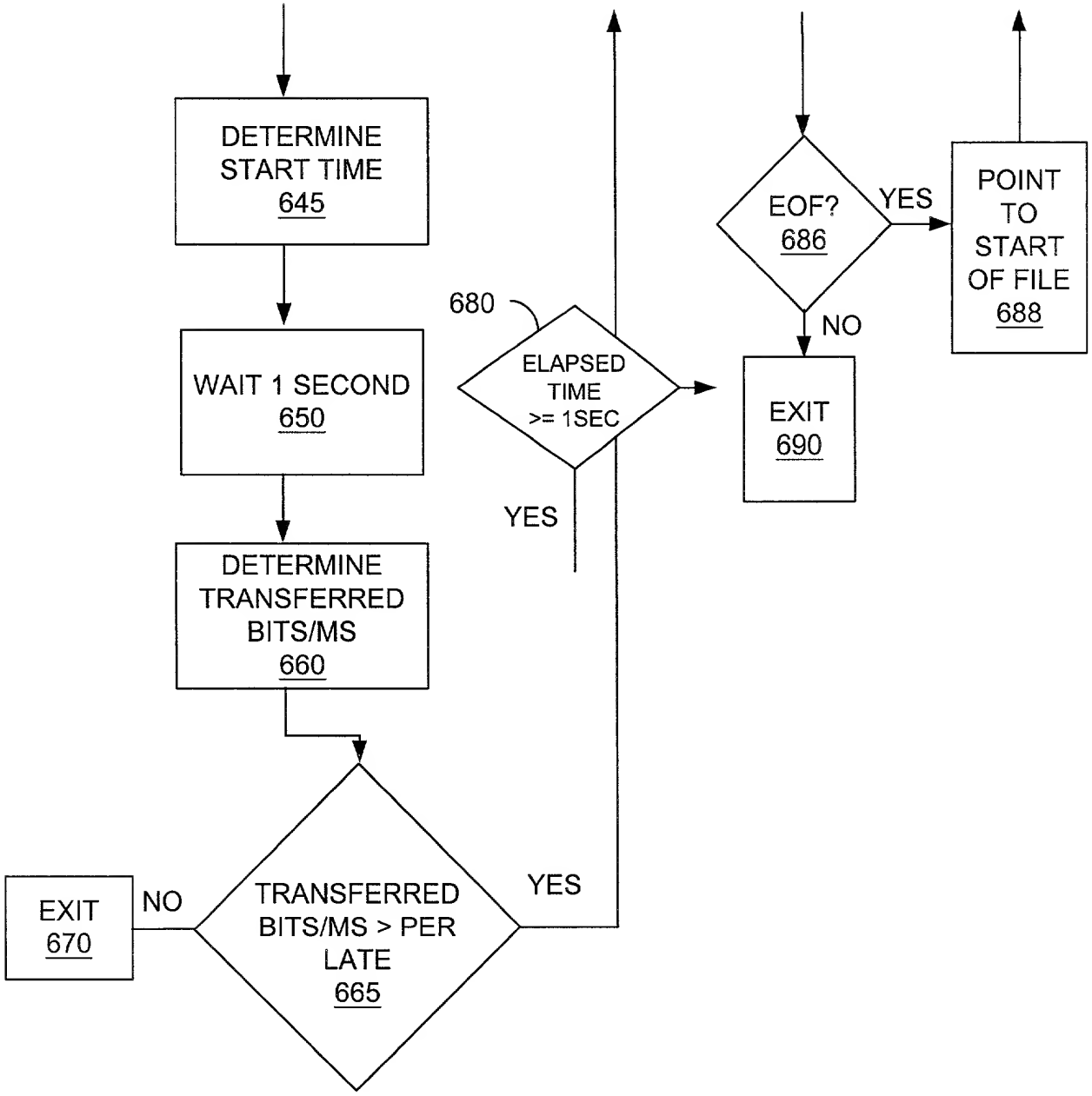
DETERMINE START TIME 645
WAIT 1 SECOND 650
DETERMINE TRANSFERRED BITS/MS 660
TRANSFERRED BITS/MS > PER LATE 665
NO
EXIT 670
YES
680
ELAPSED TIME >= 1SEC
YES
EOF? 686
YES
POINT TO START OF FILE 688
NO
EXIT 690

FIG. 6B